Study of operation of Flip Flop in the sub-threshold region in 90nm technology

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***Abstract*—This project examines the operations of a flip flop in the subthreshold region. Subthreshold operation is emerging as a good technique for low power design of circuits where speed of execution is not a primary concern.**

In this project, I aim to find the minimum energy point of a flip flop, and compare my results with the result obtained in [3].

The flip flop designed for this project is a master-slave D flip flop. The flip flop was designed in Design Architect, and the netlist was modified to 90nm technology. The simulation was done using HSPICE.

Results show that the flip flop operates perfectly in the subthreshold region of 90nm technology while providing reasonable power and energy savings.

Index Terms—master-slave flip flop, low voltage operation, very low power design, subthreshold operation.

I. Introduction

There is a growing concern with the increase in power dissipation with the scaling down of transistors. We know that Total Power (P_{total}) dissipated in a transistor consists of Static Power (P_{static}) and Dynamic Power ($P_{dynamic}$).

While the scaling down of transistors causes a reduction in dynamic power due to faster switching of the circuit, there is an increase in leakage current flowing through the circuit due to scaling down of the threshold voltages hence causing a significant increase in static power dissipation.

Hence, there is a significant interest in developing techniques for more power and energy efficient circuits at high leakage technologies.

One of the possible solutions for this conundrum is subthreshold voltage operation of circuits.

For circuit operations where execution speed is not the primary motive, the circuits can be operated at voltage below the threshold voltages of the transistors making up the circuit without losing the functionality of the circuit.

We find that scaling down the voltage gradually reduces short circuit power dissipation and it is completely eliminated at $V_{dd} \leq |V_{tp}| + V_{tn}$.

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Dynamic power is also almost completely eliminated because circuit switching is caused by leakage current flowing in the circuit and not due to the transition current.

Hence, subthreshold operation of circuits has tremendous potential in designing watches and hearing aids and in emerging ultra-low applications like distributed sensor networks [2].

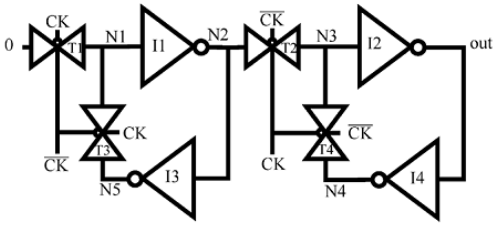
II. Circuit Modeling

Subthreshold voltage operation was performed on a master-slave D flip flop.

The circuit design used in [3] was drawn on Design Architect. The HSPICE netlist was then imported from the Design Architect simulation.

The imported netlist was modified to accommodate 90nm technology, and the technology file used was obtained from the Predictive Technology Model (PTM) website [5].

Finally, the timing and power analysis was done using HSPICE and the results were tabulated



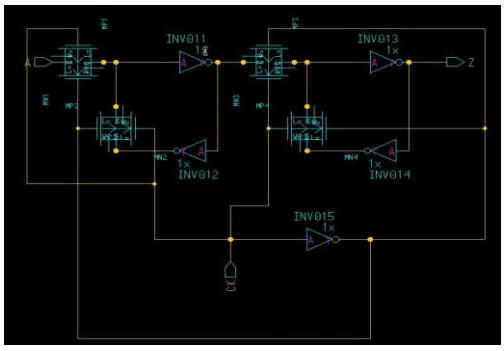


Fig. 1 [1] (Top) shows the implemented flip flop and Fig. 2 (Bottom) shows the corresponding schematic in Design Architect.

III. SIMULATION RESULTS

A. Ratioed Flip Flop

In their paper [2], Calhoun and Chandrakasan showed that a ratioed flip flop as shown in Fig. 2 will no work below 450 mV. Hence, the reason to design a more robust flip flop by cutting the feedback loops for writing the latch.

I designed the ratioed flip flop in Design Architect and simulated the voltage and energy operations at 90nm technology using HSPICE.

Fig. 3 shows that at 420mV, the flip flop fails to work. Hence, the need for a more robust design as shown in the next section is justified and actually functions in the subthreshold region.

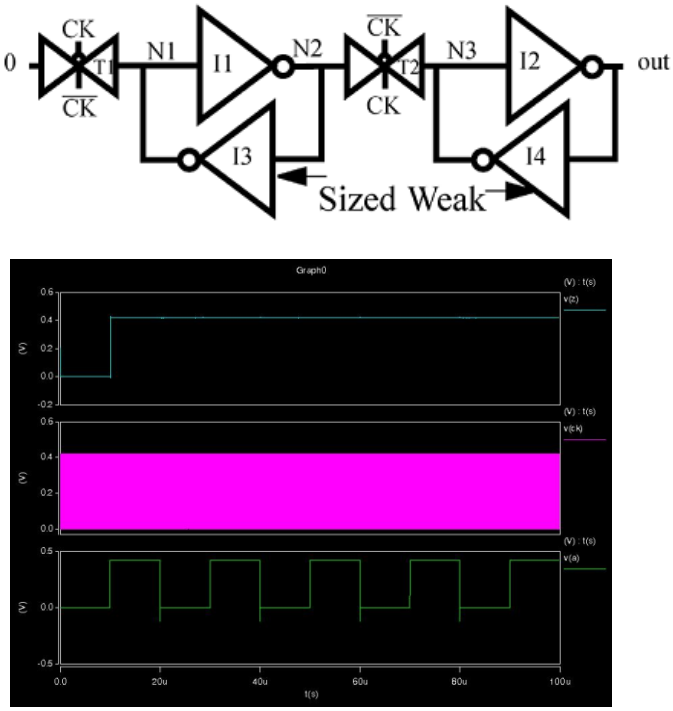


Fig. 2 (Top) shows the ratioed flip flop and (Bottom) shows the implementation in Design Architect.

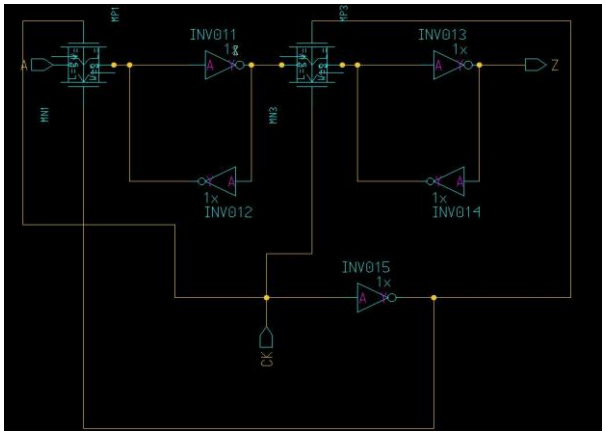


Fig. 3 shows the failure of the flip flop to drop to logic 0 at 0.42 V.

B. Flip Flop Implementation

An input of 0101 was given to the input node A of the flip flop, and the output state (Z) was noted for the input vector.

Power in the circuit was calculated by finding out how much current was drawn from the circuit during the simulation time and multiplied by the supply voltage (V_{dd}). The delay in the circuit was measured as the average of the rise and fall time delay between the input vector and the corresponding clocked output.

The energy per cycle consumed by the circuit was determined by the product of the power and the determined delay in the circuit.

The operations of the flip flop at various V_{dd} levels are tabulated below along with the power dissipation and delay at that voltage level.

Voltage (V)	Current (nA)	Power (nW)	Delay (ns)	Energy (x 10^{-18} J)
1	382	382	0.03	11.46
0.9	256	230.4	0.04	9.216
0.8	166	132.8	0.06	7.968
0.7	98.5	68.95	0.111	7.65345
0.6	68	40.8	0.185	7.548
0.5	49.9	24.95	0.29	7.2355
0.4	30.6	12.24	0.56	6.8544
0.39	29.5	11.505	0.595	6.845475
0.38	28.6	10.868	0.64	6.95552
0.35	26.1	9.135	0.815	7.445025
0.33	24.7	8.151	1.02	8.31402

Table 1 The shaded region show the voltages where we get the maximum energy savings for the flip flop.

From the table and the graph plotted in Fig. 4, we can infer that the flip flop not only works below the threshold voltage but gives us sufficient energy savings as well.

Furthermore, the timing plot in Fig. 5 shows that the output is relatively glitch free when compared with the input signal. The rise time and fall time of the input wave was set to 1ns.

The optimum voltage in normal operation mode to get the maximum energy savings is a value just above 1.1 V.

The optimum voltage at subthreshold operations for maximum energy savings is 0.39 V.

Hence, we can see that we get a higher energy savings by operating the circuit at subthreshold region (V_T = 0.397 V).

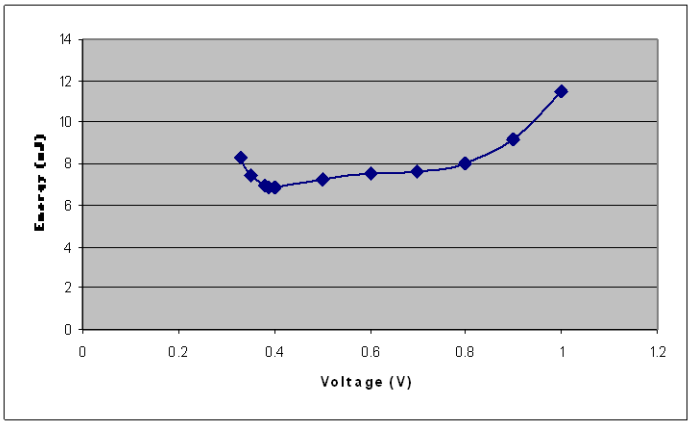


Fig. 4 plots the power x delay points given in Table 1 with respect to the voltage levels to find the optimum voltage point where we get the maximum energy savings for the flip flop.

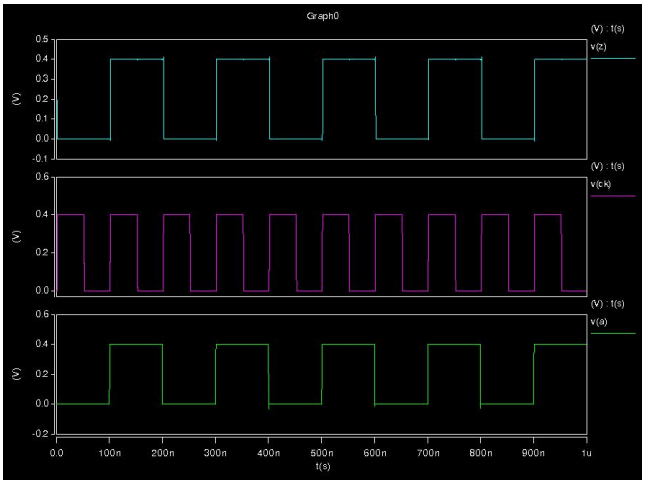


Fig. 5 shows the output of the flip flop when for the clocked signal of 0101 chain.

From Fig. 4 and Fig. 5, we can infer that the flip flop runs successfully at voltages below the threshold voltage of the circuit and the minimum energy point is situated below the threshold voltage of the circuit.

IV. CONCLUSION

This project has examined the operation of a flip flop in the subthreshold region in the 90nm technology. We have shown that the flip flop circuit can still function as its intended design when operated below the threshold voltage. The results obtained in [3] do not explicitly mention the minimum energy point of a flip flop. However, it does mention the minimum operating point of the adder circuit of which the flip flop is a part of to be 330mV. If we assume the value of the voltage to be in the same range, our result (0.397 V) is quite within the acceptable limits of error.

There are three possibilities on why this error has shown up.

Firstly, the W/L ratio of the transistors making up the flip flop is not known. Different ratios would yield different timing and power results resulting in a different minimum energy point.

Secondly, the minimum energy point changes for each individual circuit as the delay is dependant on the critical path of each circuit. More delay means the minimum energy point would shift for each circuit. Hence, 330mV would be the correct point for the 32 bit adder but incorrect for the flip flop.

Thirdly, the accuracy of the technology file used is another factor which could lead to different results. I have used the PTM model with is less accurate than the 90nm models used by Synopsis. So, a different tool would also yield to different results.

This project had three objectives. Firstly, it gave me an opportunity to look at the operations of sequential circuits in subthreshold regions. In my previous work, I had worked on combinational logics and shown their capability to operate in the subthreshold region. Furthermore, they had minimum energy points well below their threshold voltages. This project helped me prove experimentally that sequential circuits can also operate with good energy savings in the subthreshold region.

Secondly, this project gave me an opportunity to learn HSPICE and test the simulations in 90nm technology. My previous work had been restricted to 0.18um technology. This knowledge will aid me when I'm working on my thesis.

Lastly, this project has given me new insight on the operation of circuits in high leakage technologies. I will implement circuits with both sequential and combinational logic in high leakage technology and try to understand how the timing works in subthreshold regions and obtaining the minimum energy point for these circuits.

Hence, a possible future research involves modeling circuits in high leakage technologies like 65nm and below and verifying the functioning of the circuits at subthreshold voltages and checking the energy savings got at those levels.

This area has other numerous future research prospects.

Moreover, more detailed tests need to be conducted on these circuits to more accurately understand the working in the subthreshold region.

ACKNOWLEDGMENT

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